Closeout Discussion

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Cold Electronics Mini Summer School
7/21/16

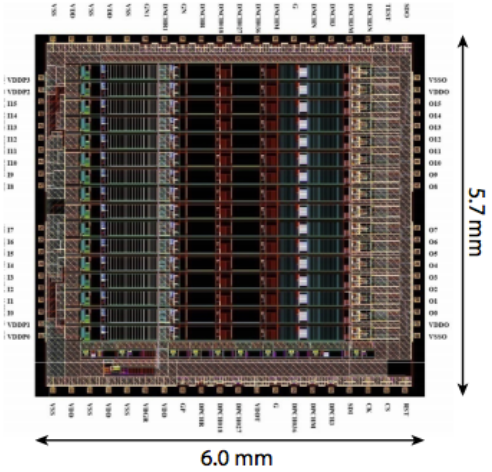
Outline

- ProtoDUNE Cold Electronics Schedule
  - Overview
  - Components
  - Teststands
- SBND/ProtoDUNE Installation
- Work to do
- Fun stuff

ProtoDUNE Schedule

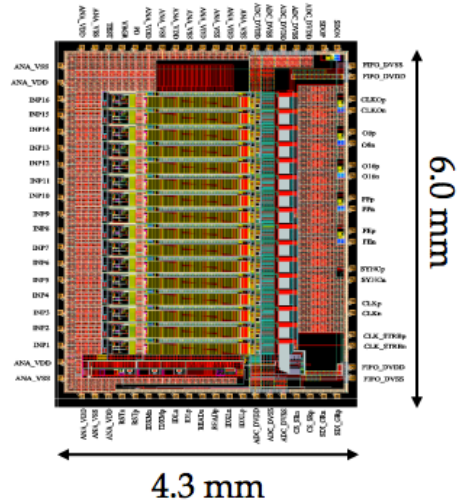
- Integration tests at FNAL/BNL/UTA: Jun 2016-…
- Vertical Slice Test (VST) at CERN: Jan-Apr 2017
- Install prototype CE on APA1 and test: May-Aug 2017
- Install CE on APA 2-6: Aug-Dec 2017
- Install APA6 into cryostat and final APA row test: Jan-Feb 2018
- Cryostat close and cooling: Feb-May 2018
- Commissioning: May-July 2018
- Data-taking with beam begins July 2018

Cold ASICs



FE

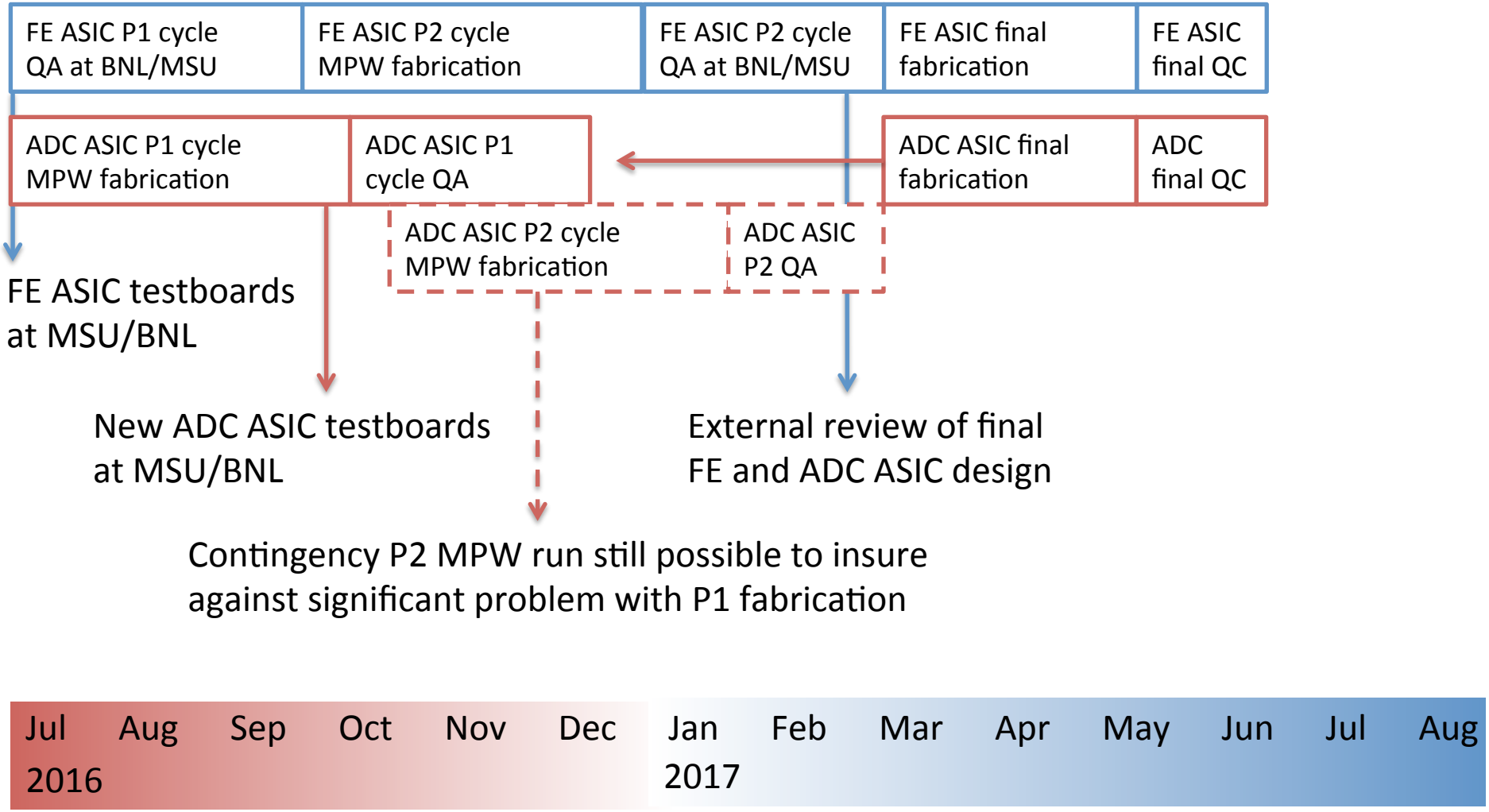
- 16 programmable channels
- Charge amplifier, filter
- Adjustable gain
  - 4.7, 7.8, 14, 25 mV/fC
- Adjustable filter time constant
  - 0.5, 1, 2, 3 µsec peaking time
- Selectable collection/non-collection wire mode
  - 200/900 mV baseline



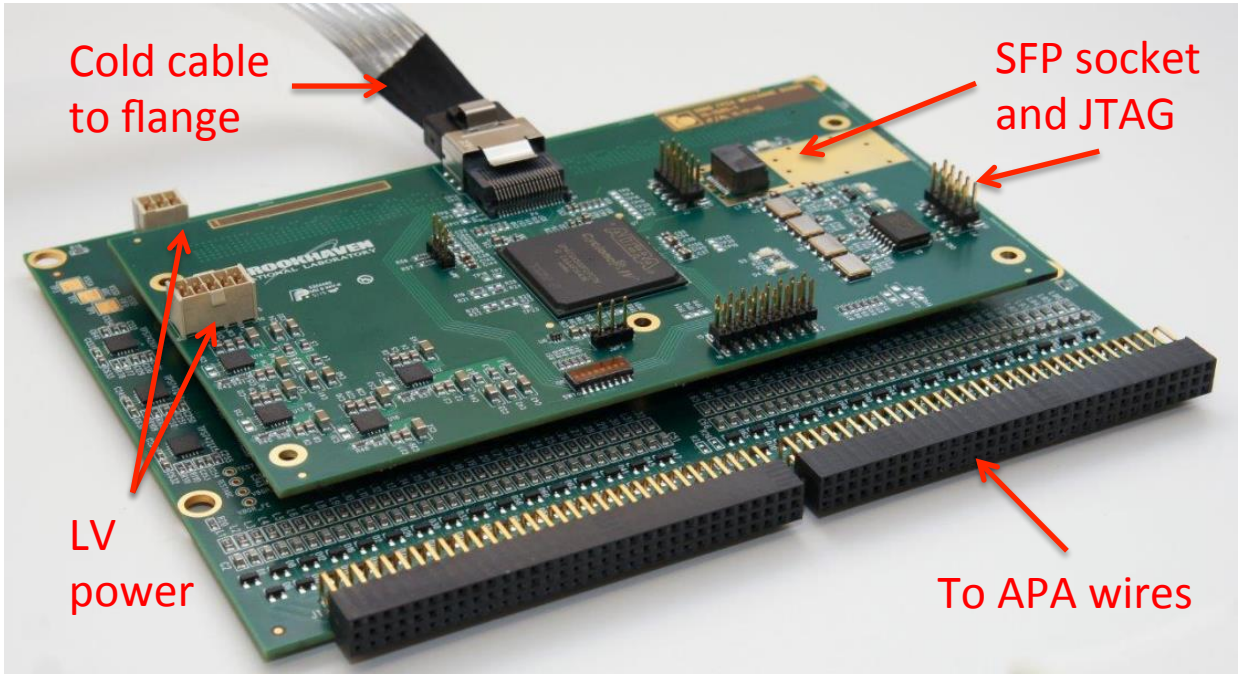
ADC

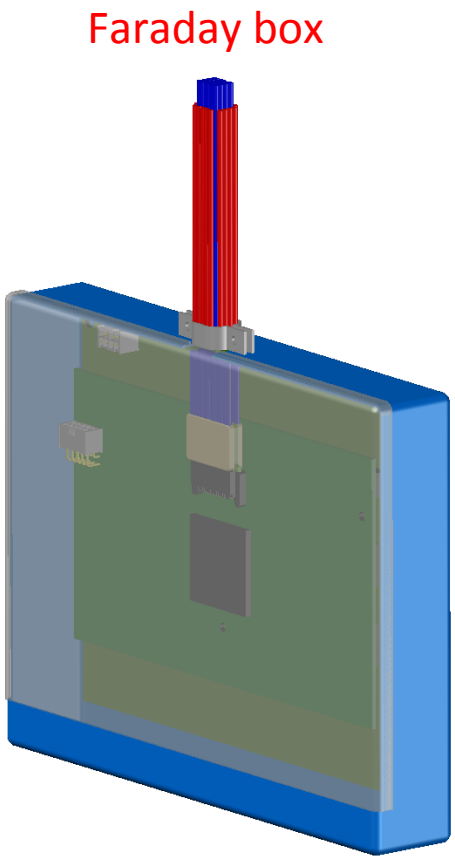
- 16 programmable channels
- 12-bit ADC sampling at 2 MHz
- ADC “stuck codes” issue in 35ton simulated and solved in next revision
  - External review Apr 7-8 was very positive
  - Expected to be sent out for MPW production by end of the month

Cold Electronics Schedule



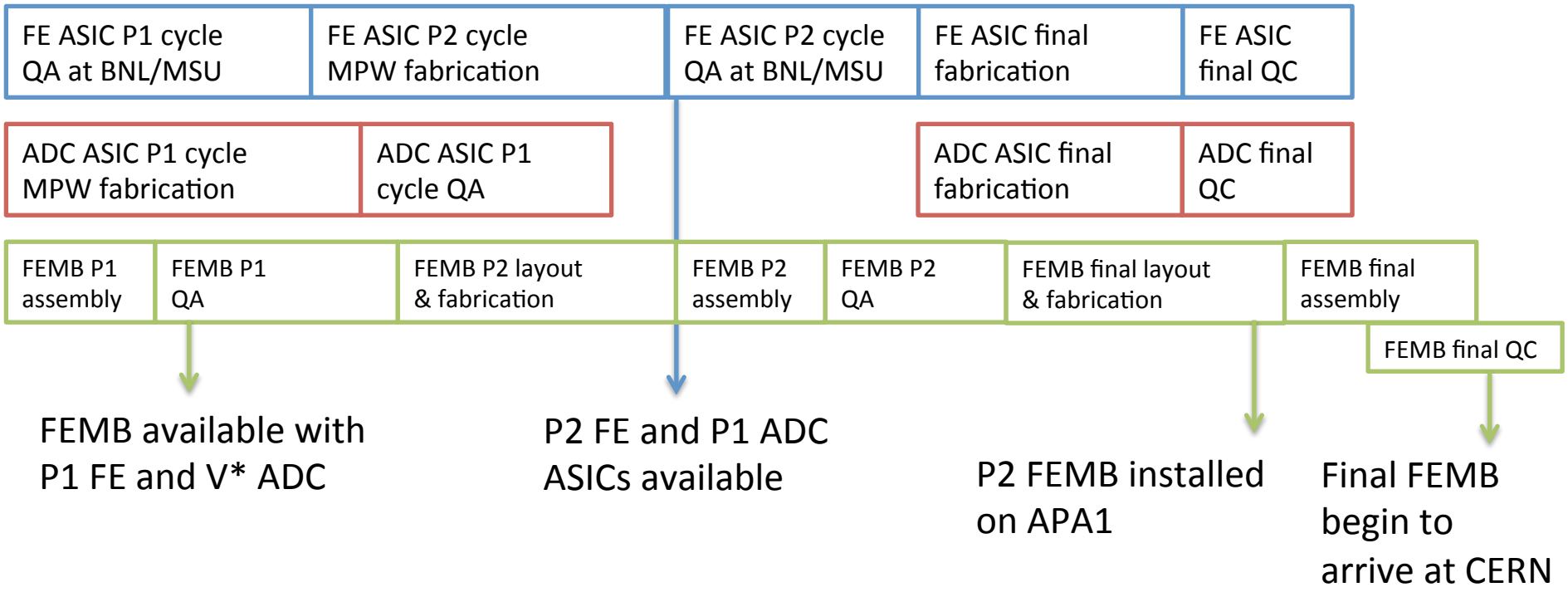
FEMB

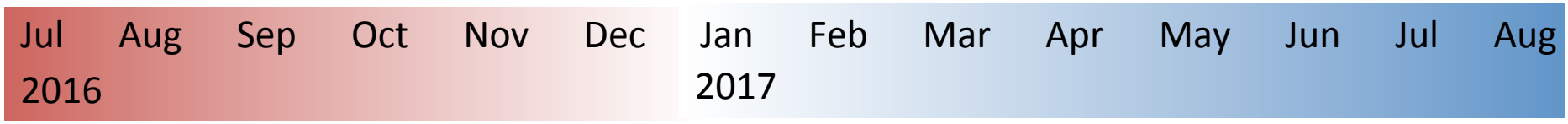




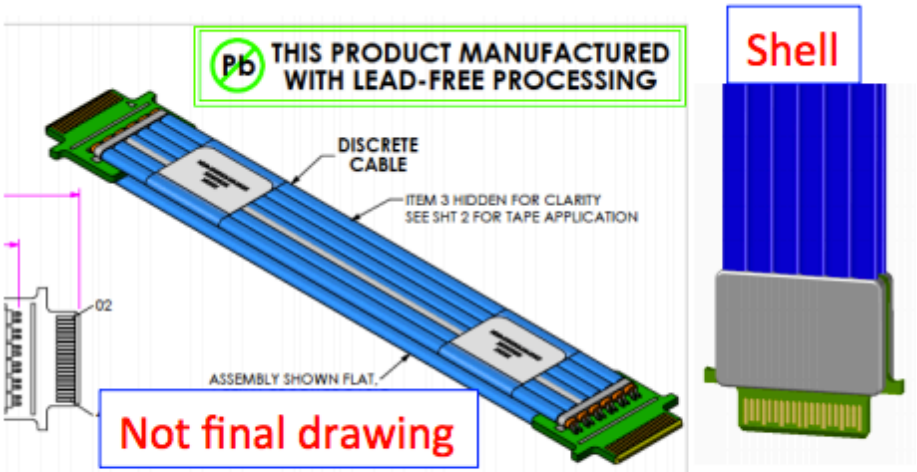
- 128 channels of digitized TPC wire readout
  - 8 FE ASICs/8 ADC ASICs on the analog motherboard
  - Controlled by 2 COLDATA/1 FPGA on the mezzanine
- Mounted in modular Faraday box with built-in cable strain relief

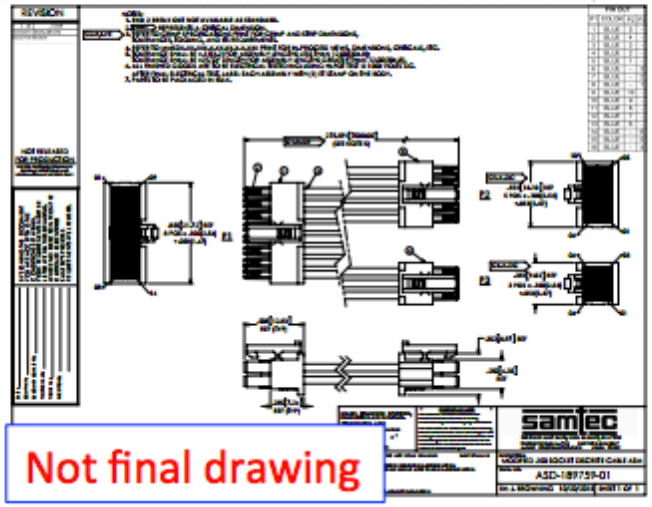
Cold Electronics Schedule





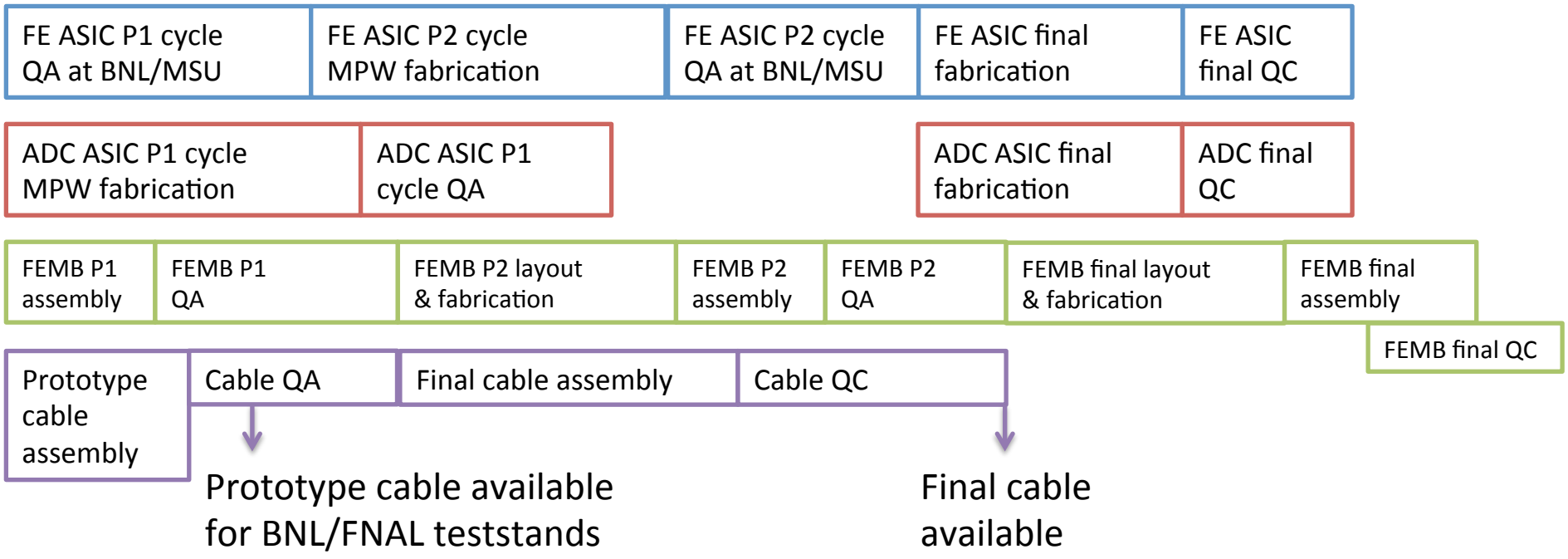
Samtec Cable Bundles



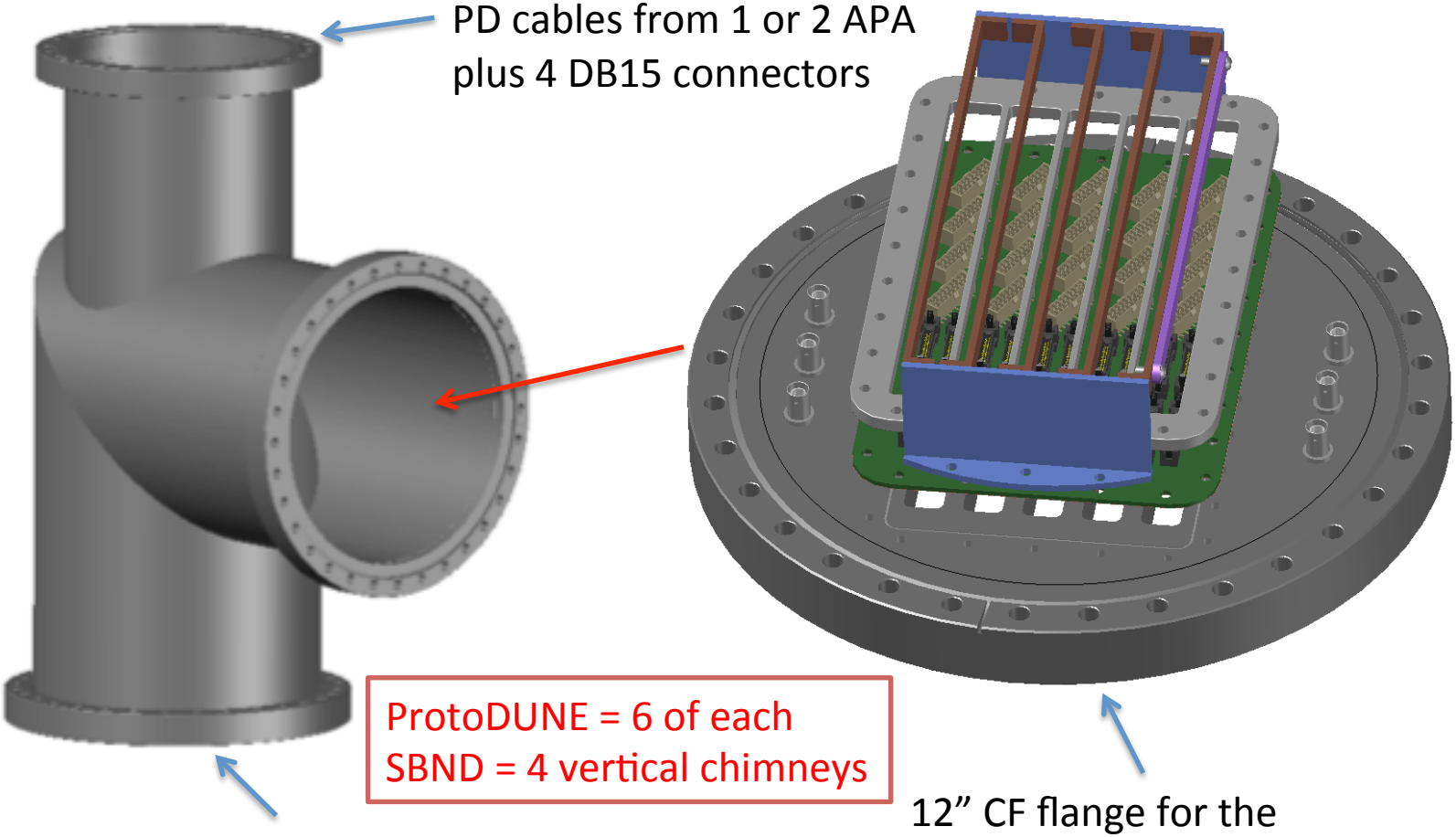


- 4 x 1.2 Gbps high-speed data links from each FEMB to the flange
- Clock, control, and FPGA programming links
- 12 pairs of Samtec 26 AWG copper twin-axial cable with THV insulation
- Samtec HSEC08 connectors to both FEMB and flange

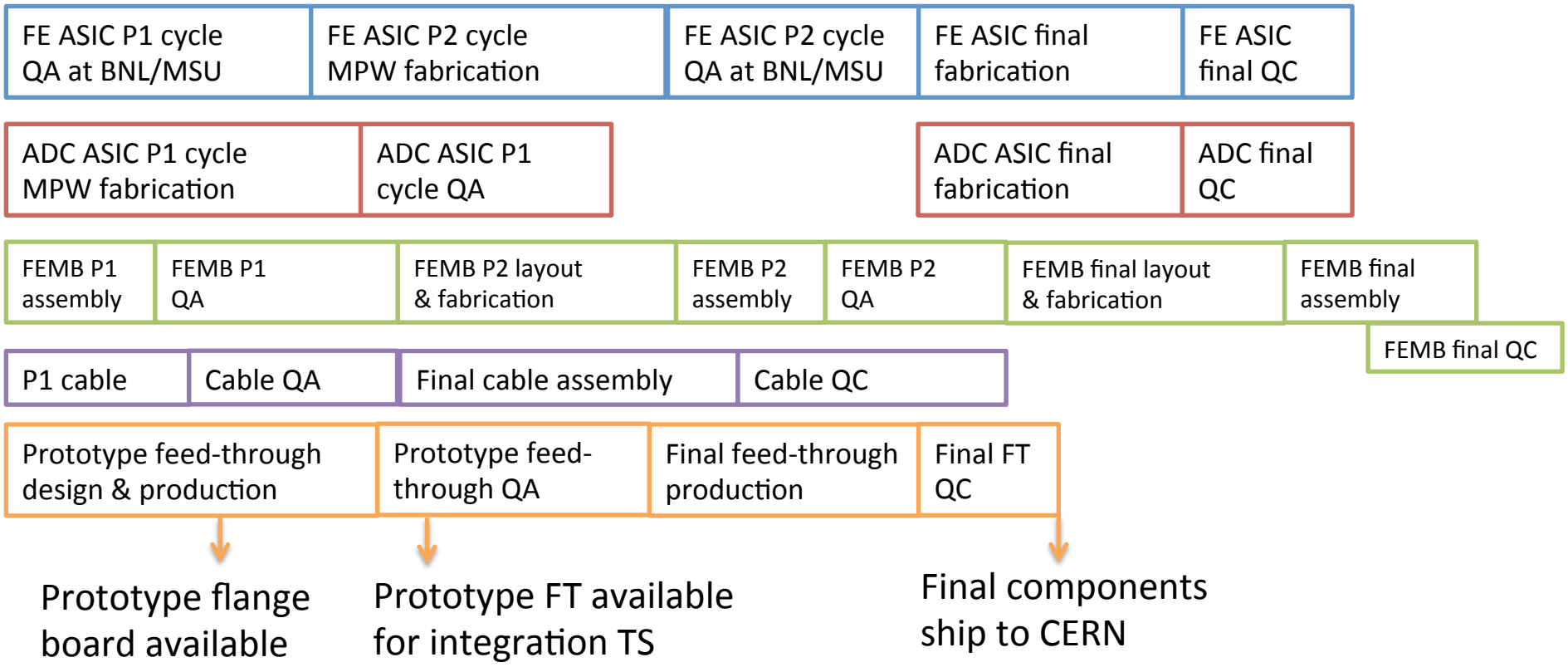
Cold Electronics Schedule



Cryostat Flange and Feed-through

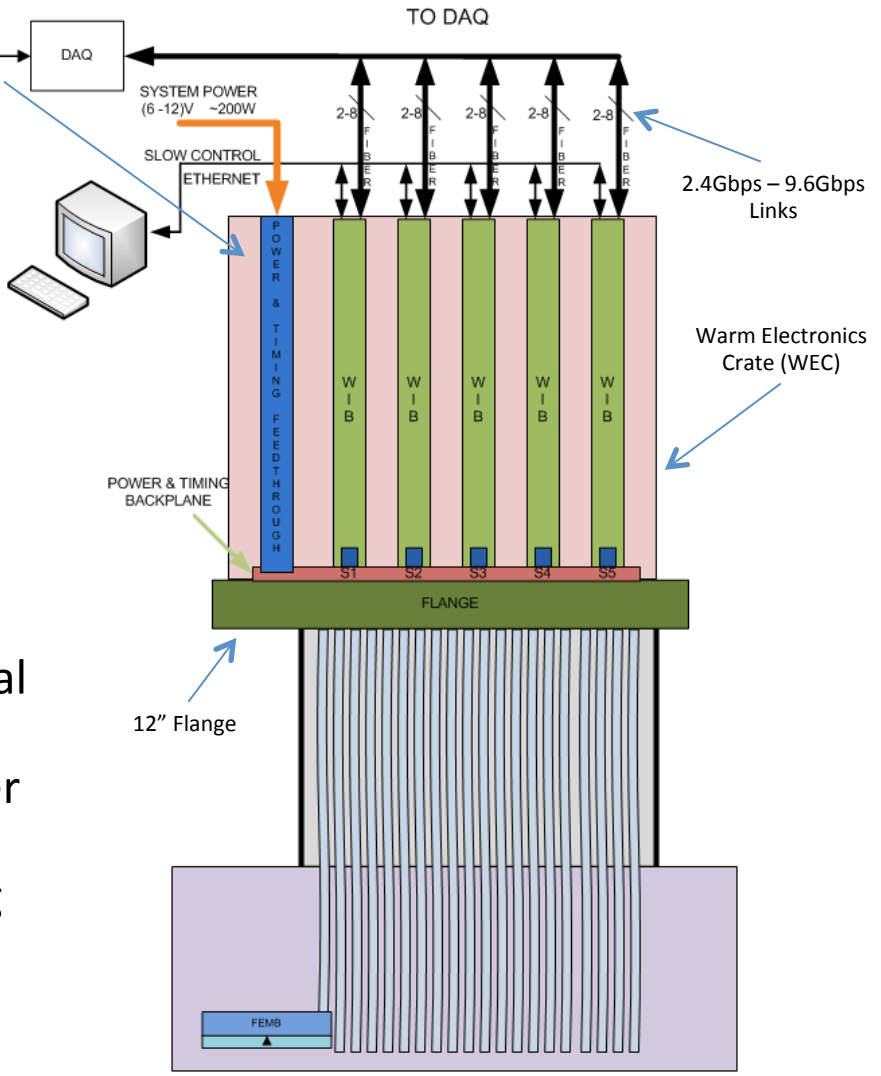


Cold Electronics Schedule



Warm Interface Electronics

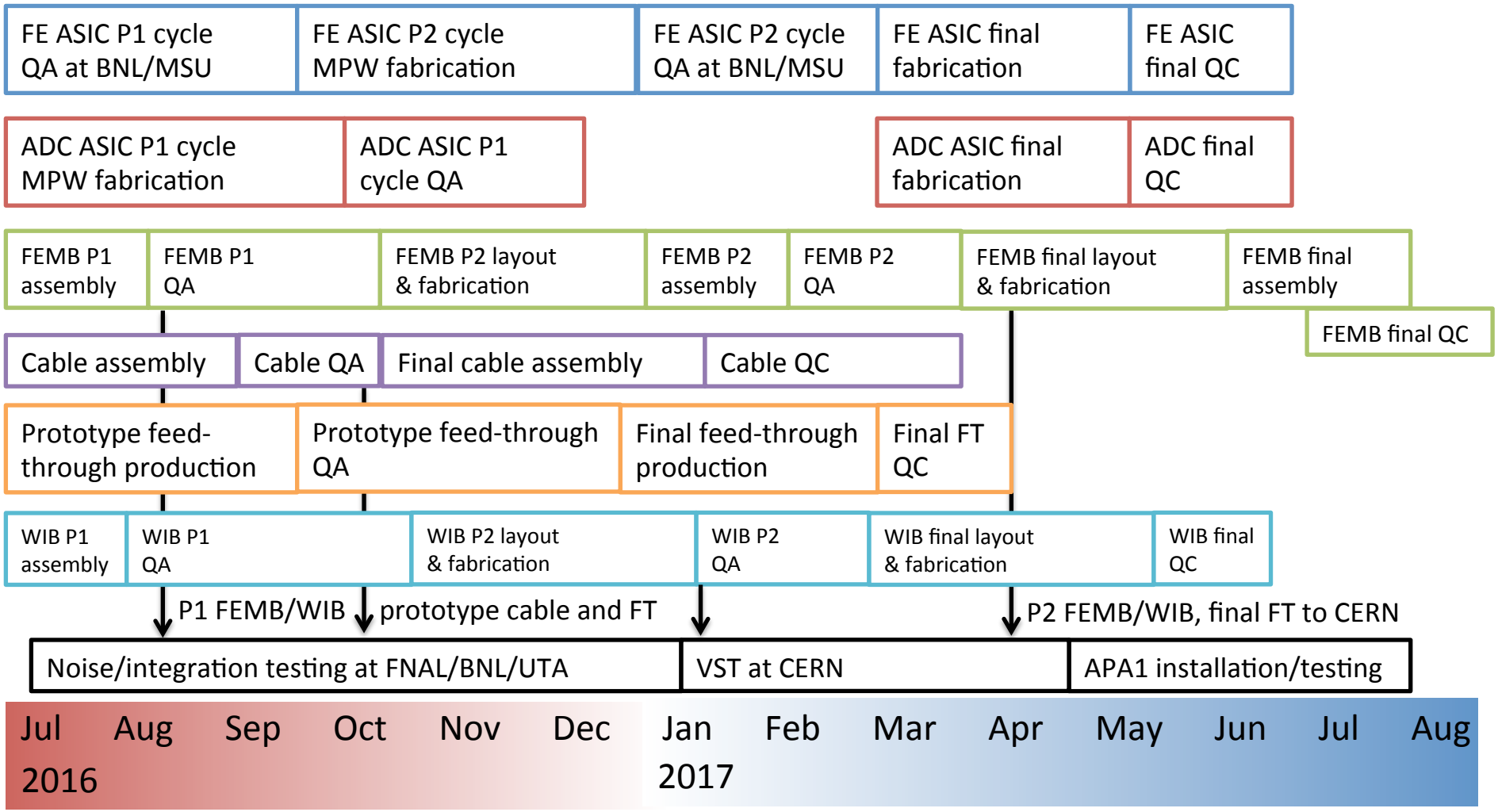
- One Warm Electronics Crate (WEC) per flange containing:
  - 5/6 Warm Interface Boards (WIB)
    - Each WIB controls up to 4 FEMBs
  - 1 Power and Timing Backplane (PTB)
  - 1 Power and Timing Card (PTC)
- Installed directly onto flange board
  - Receive high-speed data from cold cable
  - Send data to DAQ over 2-8 fiber optical links per WIB
  - Receive 50 clock and sync/control over fiber links to PTC or WIB
  - Interface to slow control system using fiber GIG-E
  - Manage power and control for FEMBs



Integration and Noise Tests

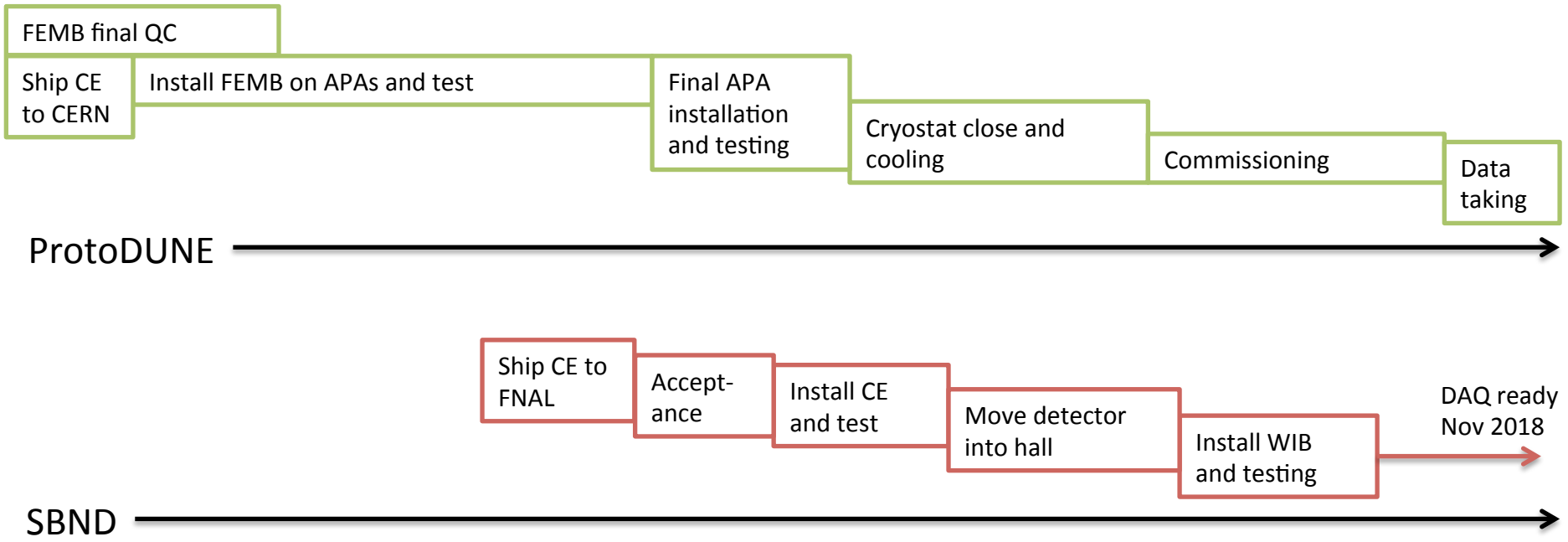
- Integration teststand at BNL
  - Full CE readout chain through the WIB
    - Multiple FEMBs, cold cable, shielded Dewar, flange+WIB
    - No wires, tests component functionality
- At Fermilab
  - SBND vertical slice teststand
  - Faraday shielded room at F0 moving to DAB for noise teststand
  - Delivering FEMB to FNAL as soon as assembled
- 40% mini-APA at BNL/CERN
  - Noise teststand at BNL using 40% mini-APA from PSL
    - Use cold, shielded box at BNL, FEMBs on wires read out by WIB
  - Mini-APA arrives this week
- Baby TPC teststand at UT Arlington
  - FEMB on wires from APA winder at UChicago
- Vertical slice teststand (VST) at CERN
  - Integration platform between cold electronics and DAQ
  - Use WIB as a CE signal generator until full CE readout chain is available to send to CERN

Cold Electronics Schedule



ProtoDUNE and SBND Installation

ASICs for SBND/ProtoDUNE are identical. All other components designed to be as functionally identical as possible.



All ProtoDUNE installation and commissioning will be complete before SBND does each of their same activities.

Jul Aug Sep Oct Nov Dec Jan Feb Mar Apr May Jun Jul Aug

2017 2018

Work to Do

- Develop component teststands
  - MSU has done a lot of work on the FE ASIC testboard and Labview
  - Penn is getting started with a 35ton FEMB
  - Python interface getting started:
    https://github.com/kirbybri/femb_udp
  - Final version ready by spring 2017
- Build integration teststands
  - Need people at BNL/FNAL to get started: in the next few months
  - Lots of hands on work with electronics when components arrive
- Validate all final components before installation
  - Bring the team together at BNL for final testing: summer 2017
- Test and install at CERN and Fermilab
  - @CERN for all of 2017, commissioning and data-taking in 2018
  - @FNAL starting at the end of 2017, installation in 2018
  - I hear Geneva is lovely in the winter…

Pictures

https://www.bnl.gov/cemss/slideshow.php

Montauk

http://www.sailingmontauk.com

Thank you!

- Lectures and Q&A:

  Xin Qian, Bo Yu, Sergio Rescia, Shaorui Li, Jack Fried, and Veljko Radeka

- Practicals and demos:

  Amanda Depoian, Jacob Larkin, Shanshan Gao, Jim Kierstead, and Brian Kirby

- Administration:

  Leisa McGee, Linda Sinatra, Chris Weaver, and Danielle Pontieri

- Organization:

  Elizabeth Worcester